REMARKS/ARGUMENTS

Claims 1-9 were pending in the Application. By this Amendment, claims 1-4 are being cancelled and claim 5 is being substantially amended to improve its form. No new matter is involved.

In Paragraph 2 on page 2 of the Final Office Action, claims 5-7 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the claims are said to contain subject matter which was not described in the Specification in such a way as to enable one skilled in the art to which it pertains or with which it is most nearly connected to make and/or use the invention. As filed, the Specification is said not to disclose "a first step of coating resin mixed with micro-particles on at least one surface of a semiconductor substrate on which a semiconductor integrated circuit is formed, and laminating a support substrate on the semiconductor substrate to hold the resin between the two substrates; and . . . wherein no connection terminals are provided between the surface of the semiconductor substrate and the support substrate . . .", as recited in independent claim 5. Claims 6 and 7 are rejected inasmuch as each includes the limitations of independent claim 5. In Paragraph 4 which begins on page 3 of the Final Office Action, claims 5-7 are further rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In the case of claim 5, the recitations ". . . a first step of coating resin mixed with micro-particles on at least one surface of a semiconductor substrate on which a semiconductor integrated circuit is formed, and laminating a support substrate on the semiconductor substrate to hold the resin between the two substrates; and . . . wherein no connection terminals are provided between the surface of the semiconductor substrate and the support substrate . . ." is said not to be understood

of how a semiconductor surface on which a semiconductor integrated circuit is formed has no connection terminals. Claims 6 and 7 are rejected on this basis inasmuch as each includes the limitations of independent claim 5.

In response, Applicant is substantially amending claim 5 in order to overcome these rejections. Claim 5 defines a method of manufacturing a semiconductor integrated device. As amended, the method of claim 5 is said to include "a first step of laminating a semiconductor substrate on which a plurality of semiconductor chips are formed and a support substrate with resin mixed with microparticles being interposed between the semiconductor substrate and the support substrate". This method includes a second step of pushing the support substrate against the semiconductor substrate. The following recitation "no connection terminals are provided between the surface of the semiconductor substrate and the support substrate" is being deleted and in its place third and fourth steps are introduced. The third step is one of "arranging wiring to achieve contact from the semiconductor chips". The fourth step is one of "dividing the semiconductor chips along scrub lines to form the semiconductor integrated device". In the final step of claim 5, in the second step the support substrate is pushed against the semiconductor substrate while keeping a distance between the semiconductor substrate and the support substrate larger than the maximum particle diameter of the microparticles.

Thus, as amended, claim 5 is submitted to be enabled by the Specification as originally filed and to be clear and definite. As amended, claim 5 is based on Fig. 3 and on the description in the Specification relating thereto.

In Paragraph 6 which begins at the bottom of page 3 of the Final Office Action, claims 1-7 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,791,168 of Connell, et al. Claims 1-4 have been cancelled. This rejection is respectfully traversed with respect to claims 5-7.

The invention of the present application relates to a chip-sized package and has the characteristic that, to fasten the semiconductor substrate having a plurality of semiconductor chips formed thereon to the support substrate by means of the resin mixed with microparticles, the support substrate is pushed against the semiconductor substrate while keeping the distance between the two substrates larger than the maximum particle diameter of the microparticles. The object to be bonded is not the semiconductor chips but rather the semiconductor substrate having a plurality of semiconductor chips formed thereon.

On the other hand, Connell, et al. discloses a method for bonding separate semiconductor chips to each other using resin and laminating the bonded semiconductor chips. Yet nowhere does the reference disclose or suggest the characteristic features in accordance with the present invention as described above.

Consequently, claim 5 as amended herein is submitted to clearly distinguish patentably over the Connell, et al. reference. Similar comments apply to claims 6 and 7 which depend from and contain all of the limitations of claim 5.

In Paragraph 1 on page 5 of the Final Office Action, claims 8 and 9 are allowed. The statement of the Examiner's reasons for allowance of such claims follows in Paragraph 2.

In conclusion, claims 5-7 are submitted to be fully enabled by the Specification, to be clear and definite, and to clearly distinguish patentably over the cited reference. Claims 8 and 9 have been allowed.

Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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